Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application--including presently cancelled claims 66, 68, 69, amended claim 67, and added new claims 82-85.

Listing of Claims:

Claim 1 (original): A semiconductor device comprising:

a layer of semiconductor material;

a thyristor formed in the layer of semi-conductor material;

the thyristor comprising at least one base-emitter junction; and

leakage species disposed in the semiconductor material and across the at least one base-emitter junction.

Claim 2 (original): The device of claim 1, in which the leakage species comprises carbon.

Claim 3 (original): The device of claim 2, in which the carbon comprises a density across the at least one base-emitter junction sufficient to establish a low-voltage leakage characteristic for the at least one base-emitter junction that is substantially greater than the leakage therefor absent the carbon.

Claim 4 (original): The device of claim 3, the low-voltage leakage characteristic greater than twice the leakage therefor absent the carbon.

Claim 5 (original): The device of claim 3, in which the low-voltage, leakage characteristic is characterized across a bias region of less than 0.50 volts.

Claim 6 (original): The device of claim 2, in which:

the at lease one base-emitter junction is defined between an anode and N-base of the thyristor;

the anode and the N-base are formed in a layer of silicon of an SOI substrate;

the N-base comprises an area per a planar top view of magnitude less than 100 x 200 nm^2; and

the carbon defines a boundary in the layer of silicon, the boundary short of the junction between the N-base and P-base of the thyristor.

Claim 7 (original): The device of claim 2, further comprising:

a layer of silicon over insulator;

the thyristor comprising N-P-N-P doped regions in the layer of silicon for the respective cathode, P-base, N-base and anode regions of the thyristor; and

each of the base-emitter junctions for the respective anode-to-N-base and cathode-to-P-base boundaries comprising carbon-silicon type defects for effecting low-level leakage.

Claim 8 (original): The device of claim 2, the density of the carbon within the at least one base-emitter junction to reduce the gain of a respective one of the bipolar transistor for the thyristor over a low-bias range therefor.

Claim 9 (original): The device of claim 8, in which the density of the carbon and an annealed structure therefor within the at least one base-emitter junction are sufficient to establish the gain of the respective bipolar transistor less than one-half a gain therefore absent the carbon.

Claim 10 (original): The device of claim 8, in which the base-emitter junction comprises a depletion width and the density of the carbon is greater than 10^{17} per $(cm)^3$ in the depletion width and less than 10^{16} per $(cm)^3$ across the base-base junction.

Claim 11 (original): A thyristor memory device, comprising:

a thyristor formed in semiconductor material, the thyristor comprising:

an anode/cathode,

a cathode/anode,

first and second base regions disposed between the anode/cathode and the cathode/anode,

a first base-emitter junction region defined between the anode/cathode and the first base region,

a second base-emitter junction region defined between the cathode/anode and the second base; and

lifetime-adjusting defects disposed within a region of the semiconductor material that includes at least a portion of a depletion region of the first base-emitter junction.

Claim 12 (original): The device of claim 11, the lifetime-adjusting defects comprising carbon-type defects.

Claim 13 (original): The device of claim 12, in which the carbon-type defects comprise an average diameter less than a nanometer.

Claim 14 (original): The device of claim 12, in which the carbon-type defects are formed by an anneal of the semiconductor material for the first base-emitter junction region with carbon disposed therein.

Claim 15 (original): The device, of claim 14, the carbon-type defects comprising a density for the carbon, and formed by an anneal, sufficient to import non-ideal I-V characteristics for the junction in at least a low voltage bias region therefor.

Claim 16 (original): The device of claim 12, in which each of the base-emitter junctions of the thyristor comprises carbon-type defects as the lifetime-adjusting defects.

Claim 17 (original): The device of claim 11, in which a bipolar transistor of the thyristor that is associated with the first base-emitter junction region comprises a gain (beta) across a low-level bias region therefor, of magnitude substantially less than an ideal gain therefor absent the lifetime-adjusting defects.

Claim 18 (original): The device of claim 11, in which the junction region between the two different base regions of the thyristor is substantially free of the lifetime-adjusting defects.

Claim 19 (original): A semiconductor memory comprising:

an access transistor comprising a gateable channel; and

a capacitively-coupled thyristor memory cell accessible via the access transistor, the capacitively-coupled thyristor comprising:

a cathode/anode region formed in semiconductor material and electrically coupled to a drain/source region of the access transistor,

at least one base-emitter junction region electrically in series with the cathode/anode, and

leakage species disposed in a region including a portion of a depletion width of the base-emitter junction region.

Claim 20 (original): The device of claim 19, in which the leakage species comprises carbon.

Claim 21 (original): The device of claim 20, in which:

the semiconductor material comprising silicon; and

the leakage species comprises C-Si self-interstitial type complexes.

Claim 22 (original): The device of claim 21, the C-Si self-interstitial type complexes comprising a density sufficient to establish a lifetime for minority carriers within the depletion width of the base-emitter junction region of magnitude substantially less than that for intrinsic silicon.

Claim 23 (original): The device of claim 22, in which the C-Si self-interstitial type complexes form "micro" defects within the silicon lattice associated with the depletion width of the base-emitter junction region.

Claim 24 (original): The device of claim 23, in which the micro defects comprise an average diameter less than one nanometer.

Claims 25-65 (withdrawn).

Claim 66 (currently cancelled).

Claim 67 (currently amended): A thyristor semiconductor memory device comprising:

a thyristor comprising anode-emitter and cathode-emitter regions and two separate base regions of opposite type conductivity between the anode-emitter region and the cathode-emitter region;

an electrode capacitively-coupled to one of the two base regions; and

a shunt to shunt low-level current of at least one of the base regions, comprising:

a transistor having source and drain regions;

one of the source and drain regions electrically coupled to one of the cathode and

anode regions of the thyristor;

the other of the source and drain regions being electrically coupled to one of the two base regions; and

the transistor further comprising a gate electrically coupled to the other of the two base regions and operable under bias to control a conductivity between the source and drain regions.

Claims 68-69 (currently cancelled).

Claims 70-81 (withdrawn).

Claim 82 (new): The semiconductor device of claim 2, in which the carbon within the at least one base-emitter junction causes a reduction in a bipolar gain of the thyristor.

Claim 83 (new): The semiconductor device of claim 82, in which current flows across the at least one base-emitter junction and the reduction in gain is greater at lower current levels than at higher current levels.

Claim 84 (new): The semiconductor device of claim 67, in which:

the transistor comprises a MOSFET;

the source/drain region of the MOSFET electrically coupled to the cathode region of the thyristor;

the drain/source region of the MOSFET electrically coupled to the p-base region of the thyristor; and

the gate of the MOSFET electrically coupled to the n-base region of the thyristor.

Claim 85 (new): The semiconductor device of claim 67, in which:

the transistor comprises a MOSFET defined in part by the source region, the drain region and the gate;

the drain/source region of the MOSFET electrically coupled to the anode region of the thyristor;

the source/drain region of the MOSFET electrically coupled to the n-base region of the thyristor; and

the gate of the MOSFET electrically coupled to p-base region of the thyristor.